What is claimed is:

1. Apparatus comprising:

a computer system having

a central processing unit,

memory elements operatively coupled to said central processing unit, and

an option bus operatively coupled to said central processing unit and said memory elements; and

a network processor option card operatively connected to said computer system through said option bus, said option card having mounted thereon:

a plurality of interface processors;

instruction memory storing instructions accessibly to said interface processors;

data memory storing data passing through said option card from said memory elements and accessibly to said interface processors; and

a plurality of input/output ports;

one of said input/output ports exchanging data passing through said option card with an external network under the direction of said interface processors;

said option card cooperating with said computer system in directing the exchange of data between said data exchange input/output ports and the flow of data through said data memory to and from said memory elements in response to execution by said interface processors of instructions loaded into said instruction memory and providing pattern recognition services for the flow of data.

2. Apparatus according to Claim 1 wherein said interface processors, said instruction memory, said data memory and said input/output ports are comprised within a network processor.

3. Apparatus according to Claim 2 wherein said network processor comprises a semiconductor substrate and further wherein said interface processors, said instruction memory, said data memory and said input/output ports are formed on said semiconductor substrate.

4. Apparatus according to Claim 1 wherein the number of said interface processors exceeds four.

5. Apparatus according to Claim 1 wherein said option card analyses bit strings for the presence of predetermined indicator bit sequences.

6. Apparatus according to Claim 5 wherein said option card analyses bit strings for virus signatures.

7. Apparatus according to Claim 5 wherein said option card selects portions of bit strings to be passed to said computer system based upon the determined presence of predetermined indicator bit sequences.

8. Apparatus according to Claim 5 wherein said option card selects portions of bit strings to be barred from passage to said computer system based upon the determined presence of predetermined indicator bit sequences.

9. Apparatus according to Claim 5 wherein the analysis of bit strings proceeds at the speed of data flow to said option card.

10. Apparatus comprising:

a plurality of a computer systems each having

a central processing unit, and

server memory;

a network processor coupled to each of said computer systems and joining

the coupled computer systems into a server farm, said network processor having

a plurality of interface processors;

instruction memory storing instructions accessibly to said interface processors;

data memory storing data passing through said network processor to and from each of said coupled computer systems accessibly to said interface processors; and

a plurality of input/output ports;

one of said input/output ports exchanging data passing through said network processor with an external network under the direction of said interface processors;

others of said input/output ports exchanging data passing through said network processor with said coupled computer systems;

said network processor cooperating with said coupled computer systems in directing the exchange of data between said input/output ports and the flow of data through said data memory to and from said coupled computer systems in response to execution by said interface processors of instructions loaded into said instruction memory and providing pattern recognition services for the flow of data.

11. Apparatus according to Claim 10 wherein said network processor comprises a semiconductor substrate and further wherein said interface processors, said instruction memory, said data memory and said input/output ports are formed on said semiconductor substrate.

12. Apparatus according to Claim 11 wherein the number of said interface processors exceeds four.

13. Apparatus according to Claim 10 wherein said network processor analyses

bit strings for the presence of predetermined indicator bit sequences.

14. Apparatus according to Claim 13 wherein said network processor analyses bit strings for virus signatures.

15. Apparatus according to Claim 13 wherein said network processor selects portions of bit strings to be passed to said computer systems based upon the determined presence of predetermined indicator bit sequences.

16. Apparatus according to Claim 13 wherein said network processor selects portions of bit strings to be barred from passage to said computer systems based upon the determined presence of predetermined indicator bit sequences.

17. Apparatus according to Claim 10 wherein the analysis of bit strings proceeds at the speed of data flow to said network processor.

18. A computer system comprising:

a central processing unit;

a plurality of DASD peripheral devices operatively associated with said central processing unit; and

a network processor operatively interposed between said central processing unit and said DASD peripheral devices and among said DASD peripheral devices, said network processor having

a plurality of interface processors;

instruction memory storing instructions accessibly to said interface processors;

data memory storing accessibly to said interface processors data passing through said network processor from and to said DASD peripheral devices; and

a plurality of input/output ports exchanging data passing through said

network processor with said DASD peripheral devices;

said network processor cooperating with said central processing unit in directing the exchange of data between said input/output ports and the flow of data through said data memory to and from said DASD peripheral devices in response to execution by said interface processors of instructions loaded into said instruction memory and providing pattern recognition services for the flow of data.

19. Apparatus according to Claim 18 wherein said network processor comprises a semiconductor substrate and further wherein said interface processors, said instruction memory, said data memory and said input/output ports are formed on said semiconductor substrate.

20. Apparatus according to Claim 19 wherein the number of said interface processors exceeds four.

21. Apparatus according to Claim 18 wherein said network processor analyses bit strings for the presence of predetermined indicator bit sequences.

22. Apparatus according to Claim 21 wherein said network processor analyses bit strings for virus signatures.

23. Apparatus according to Claim 21 wherein said network processor selects portions of bit strings to be passed to a receiving one of said computer system and said DASD peripheral devices based upon the determined presence of predetermined indicator bit sequences.

24. Apparatus according to Claim 21 wherein said network processor selects portions of bit strings to be barred from passage to a receiving one of said computer system and said DASD peripheral devices based upon the determined presence of predetermined indicator bit sequences.

25. Apparatus according to Claim 18 wherein the analysis of bit strings proceeds at the speed of data flow to said network processor.